The Circuit Designer's Companion: Power supply returns & I/O signal grounding

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电路设计师指导手册（2）：电源返回路径与 I/O 信号接地

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[Part 1 began a look at grounding: when to consider it, how chassis materials affect it, and the problem of ground loops.]

[第一部分开始对接地有了初步了解：何时考虑接地，机箱材料如何影响接地，以及接地环路问题]

1.1.5 Power supply returns

You will note from Figure 1.2 that the output power supply 0 V connection (0 V(B)) has been shown separately from 0 V(A), and linked only at the power supply itself. What happens if, say for reasons of economy in wiring, you don't follow this practice but instead link the 0 V rails together at PCB3 and PCB2, as shown in Figure 1.6.

1.1.5 电源返回路径

从图 1.2 可以看出，输出电源 0V 连线(0V(B))是与 0V(A)分开的，只在电源本身上有链接。如果比方说因为走线经济方面的原因，你没有按照这个操作，而是在 PCB3 和 PCB2 处将 0V 轨接在一起，如图 1.6 所示，将会发生什么情况呢？

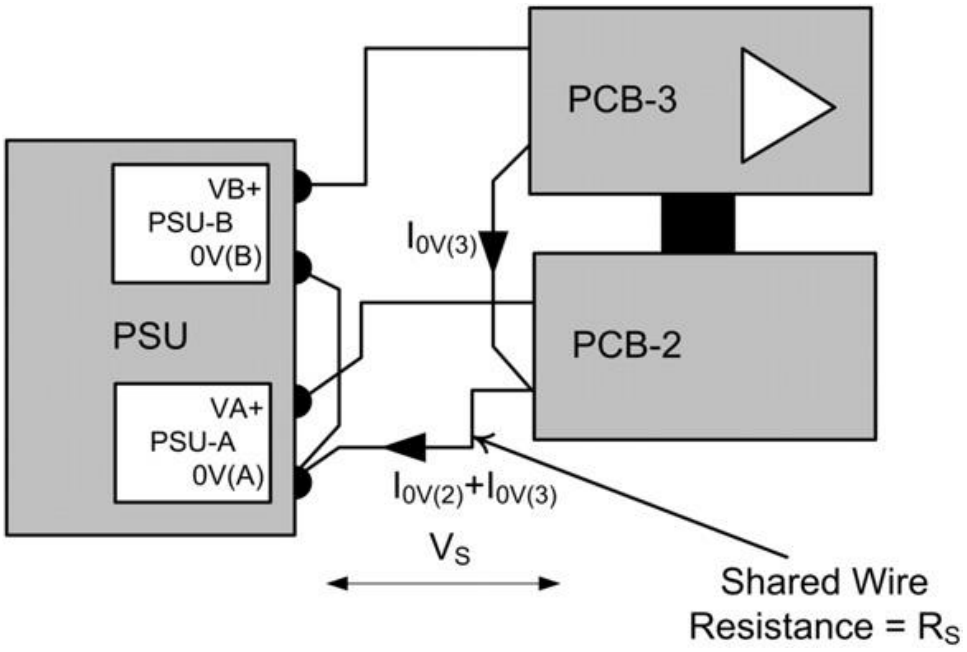

FIGURE 1.6 Common power supply return

图 1.6：公共电源返回路径。

The supply return currents I_{0V} from both PSUB/PCB3 and PSUA/PCB2 now share the same length of wire (or track, in a single-PCB system). This wire has a certain non-zero impedance, say for DC purposes it is R_S. In the original circuit this was only carrying $I_{0V(2)}$ and so the voltage developed across it was:

来自 PSUB/PCB3 和 PSUA/PCB2 的电源返回电流 I_{0V} 现在共享相同长度的导线(或单块 PCB 系统中的走线)。这根导线显著具有某个非零的阻抗，比如出于直流目的其值为 R_S。在原始电路中，这根导线只承载 $I_{0V(2)}$，因此上面产生的电压是：

$$V_S = R_S \times I_{0V(2)}$$

but, in the economy circuit,
但在经济型电路中，

$$V_S = R_S \times (I_{0V(2)} + I_{0V(3)})$$

This voltage is in series with the supply voltages to both boards and hence effectively subtracts from them. Putting some typical numbers into the equations,

这个电压与连接两块电路板的电源电压串联在一起，因此要从电源电压中减去这个值。将一些典型数值代入公式，

$I_{0V(3)}$ = 1.2 A with a VB+ of 24 V because it is a high-power output board;

$I_{0V(2)}$ = 50 mA with a VA+ of 3.3 V because it is a microprocessor board with some CMOS logic on it:

VB+为 24V 时，$I_{0V(3)}$ = 1.2 A，因为它是一个大功率输出电路板；
VA+为 3.3V 时，$I_{0V(2)}$ = 50 mA，因为它是一个微处理器板，上面有一些 CMOS 逻辑：

Now assume that, for various reasons, the power supply is some distance remote from the boards and you have without thinking connected it with 2 m of 7/0.2 mm equipment wire, which will have a room temperature resistance of about 0.2 Ω. The voltage V_S will be

现在假设，因为多种原因，电源与电路板有一定的距离，你只能用 2 米长的 7/0.2mm 设备导线连接,这根导线在室温下的电阻约为 0.2Ω。那么电压 V_S将是：

$$V_S = 0.2 \times (1.2 + 0.05) = 0.25 \text{ V}$$

which will drop the supply voltage at PCB2 to 3.05 V, less than the lower limit of operation for 3.3 V logic, *before* allowing for supply voltage tolerances and other voltage drops. One wrong wiring connection can make your circuit operation borderline! Of course, the 0.25 V is also subtracted from the 24 V supply, but a reduction of about 1% on this supply is unlikely to affect operation.

在虑及供电电压容差和其它压降之前，上述导线将使 PCB2 上的电源电压下降到 3.05V，低于 3.3V 逻辑电路工作的下限。一种错误的导线连接将使你的电路工作岌岌可危！当然，也要从 24V 电源中减去 0.25V，但这个电源减小约 1%基本上不会影响到正常工作。

Varying loads

If the 1.2 A load on PCB3 is varying – say several high-current relays may be switched at different times, ranging from all off to all on – then the V_S drop at PCB2 would also vary. This is very often worse than a static voltage drop because it introduces noise on the 0 V line. The effects of this include unreliable processor operation, variable set threshold voltage levels and odd feedback effects such as chattering relays or, in audio circuits, low-frequency "motor-boating" oscillation.

不断改变的负载

如果PCB3上的1.2A负载在变化——比方说几个大电流继电器可能在不同时间切换，从全关到全开——那么 PCB2 上的 V_S压降也会发生变化。这种情况通常比静态压降要糟糕，因为它会在 0V 线上引入噪声，最终造成的后果包括：处理器工作不可靠,设置的电压阈值发生变化,以及奇怪的反馈效应,比如继电器的颤动，或者在音频电路中产生低频“次声频”振荡。

For comparison, look at the same figures but applied to Figure 1.2, with separate 0 V return wires. Now there are two voltage drops to consider: $V_{S(A)}$ for the 3.3-V supply and $V_{S(B)}$ for the 24-V supply. $V_{S(B)}$ is 1.2 A times 0.2 Ω, substantially the same (0.24 V) as before, but it is only subtracted from the 24-V supply. $V_{S(A)}$ is now 50 mA times 0.2 Ω or 10 mV, which is the only 0 V drop on the 3.3-V supply to PCB2 and is negligible. The rule is: always separate power supply returns so that load currents for each supply flow in separate conductors (Figure 1.7).

为了进行比较，将相同的数字应用于图 1.2，并且采用分开的 0V 返回线。现在有两个压降需要考虑：针对 3.3V 电源的 $V_{S(A)}$和针对 24V 电源的 $V_{S(B)}$。$V_{S(B)}$是 1.2A 乘上 0.2Ω的值，与前面算的值(0.24V)相同，但只从 24V 电源中减掉。现在 $V_{S(A)}$是 50mA 乘以 0.2Ω，或 10mV，对于 PCB2 的 3.3V 电源来说压降几乎是 0V，可以忽略。规则是：每次都要把电源返回路径分开来，以便每个电源的负载电流在分开的导体中流动(图 1.7)。

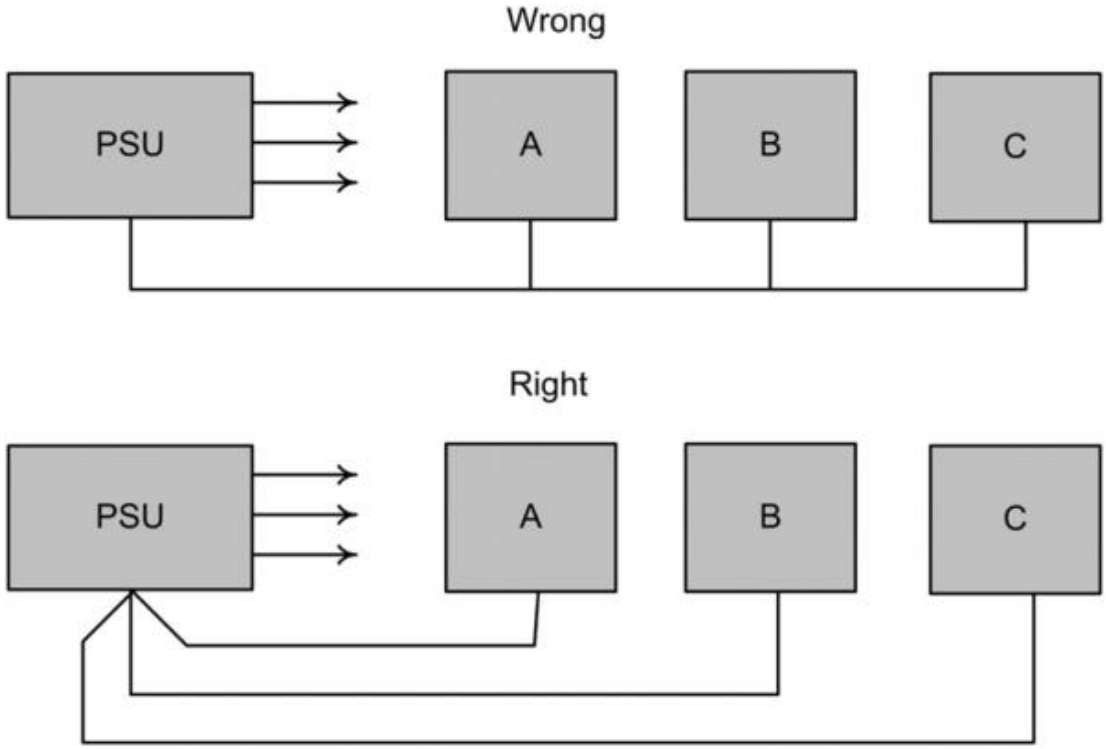

FIGURE 1.7 Ways to connect power supply returns

图 1.7 连接电源返回路径的方式。

Note that this rule is easiest to apply if different power supplies have different 0 V connections (as in Figure 1.2) but should also be applied if a common 0 V is used, as shown above. The extra investment in wiring is just about always worth it for peace of mind!

值得注意的是，当不同电源具有不同的 0V 线(如图 1.2 中所示)时，这个规则最容易满足。但是，如果使用公共的 0V 线，上述规则也应该满足，如上图所示。为求内心的平静，对布线的额外付出总是值得的。

Power rail feed

The rule also applies to the power rail feed as well as to its return, and in fact to any connection where current is being shared between several circuits. Say the high-power load on PCB3 was also being fed from the +5 V supply VA+, then the preferred method of connection is two separate feeds (Figure 1.8).

电源轨馈线

上述规则同样适用于电源轨馈线及其返回路径，事实上当电流要在多个电路之间共享时任何连接都要满足这个规则。比方说 PCB3 上的大功率负载也从+5V 电源 VA+得到供电，那么更好的连接方法是两个分开的馈电线(图 1.8)。

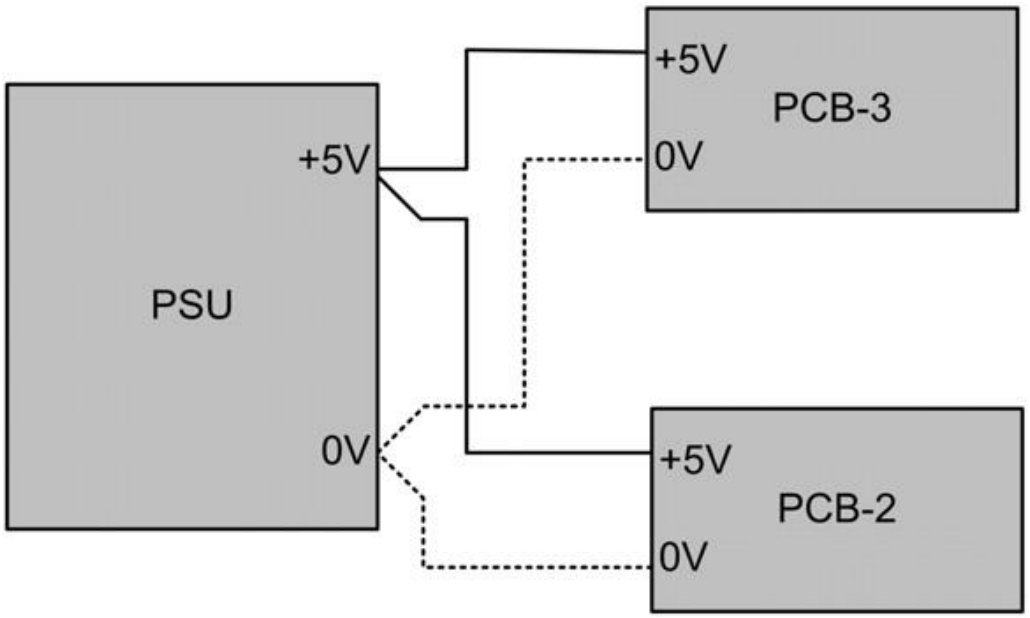

FIGURE 1.8 Separate power supply rail feeds

图 1.8:分开的电源轨馈线。

The reasons are the same as for the 0 Vreturn: with a single feed wire, a common voltage drop appears in series with the supply voltage, injected this time in the supply rail rather than the 0 V rail. Fault symptoms are similar.

这样的理由与 0V 返回路径是相同的：当采用单根供电线时，会出现与供电电压串联的公共压降，这次这个压降是注入电源轨而不是 0V 轨。故障症状也是相似的。

Of course, the example above is somewhat artificial in that you would normally use a rather more suitable size of wire for the current expected.

High currents flowing through long wires demand a low-resistance and hence a thick conductor is required. If you are expecting a significant voltage drop then you will take the trouble to calculate it for a given wire diameter, length and current. See Table 1.3 on page 24 for a guide to the current-carrying abilities of common wires. The point of the previous examples is that voltage drops have a habit of cropping up when you are *not* expecting them.

当然，上述例子多少是有些人为的，因为为了得到期望的电流通常要使用尺寸更加合适的导线。在长导线中流经大电流要求低的电阻，因此要求使用厚的导体。如果你预测有显著的压降，那么你就得劳烦计算在给定线径、长度和电流条件下的压降值。第 24 页上的表 1.3 给出了普通导线的电流承载能力供参考。前面这个例子的要点是，压降具有当你不希望见到它们时突然出现的习惯。

Conductor impedance

Note that the previous examples, and those on the next few pages, tacitly assume for simplicity that the wire impedance is resistive only. In fact, real wire has inductance as well as resistance and this comes into effect as soon as the wire is carrying AC, increasing in significance as the frequency is raised.

导体阻抗

需要注意的是，在前面的例子以及后面几页的例子中，为了简单起见，都假设导线阻抗是纯电阻。事实上，实际的导线既有电阻也有电感，当导线承载交流信号时电感就会起使用，并且随着信号频率的增加电感效应愈加明显。

A one-meter length of 16/0.2 equipment wire has a resistance of 38mΩ and a self-inductance of 1.5 μH. At 4 A DC the voltage drop across it will be 152mV. An AC current with a rate of change of 4 A/μs will generate 6 V across it. Note the difference! The later discussion of wire types includes a closer look at inductance.

一米长的 16/0.2 规格设备导线具有 38mΩ 的电阻和 1.5μH 的自感量。在流经 4A 直流电流时，这段导线上的压降为 152mV。而变化率为 4 A/μs 的交流电流将在上面产生 6V 的电压。注意这个差别是很大的！后面对导线类型的讨论包含了详细的电感方面内容。

1.1.6 Input signal ground

Figure 1.2 shows the input signal connections being taken directly to PCB1 and not grounded outside of the PCB. To expand on this, the preferred scheme for two-wire single-ended input connections is to take the ground return directly to the reference point of the input amplifier, as shown in Figure 1.9(a).

1.1.6 输入信号地

图 1.2 显示输入信号被直接连线到了 PCB1，没有在 PCB 外面接地。为了在此基础上作进一步扩展，两线单端输入连接的优选方案是将接地回路直接接到输入放大器的参考点，如图 1.9(a)所示。

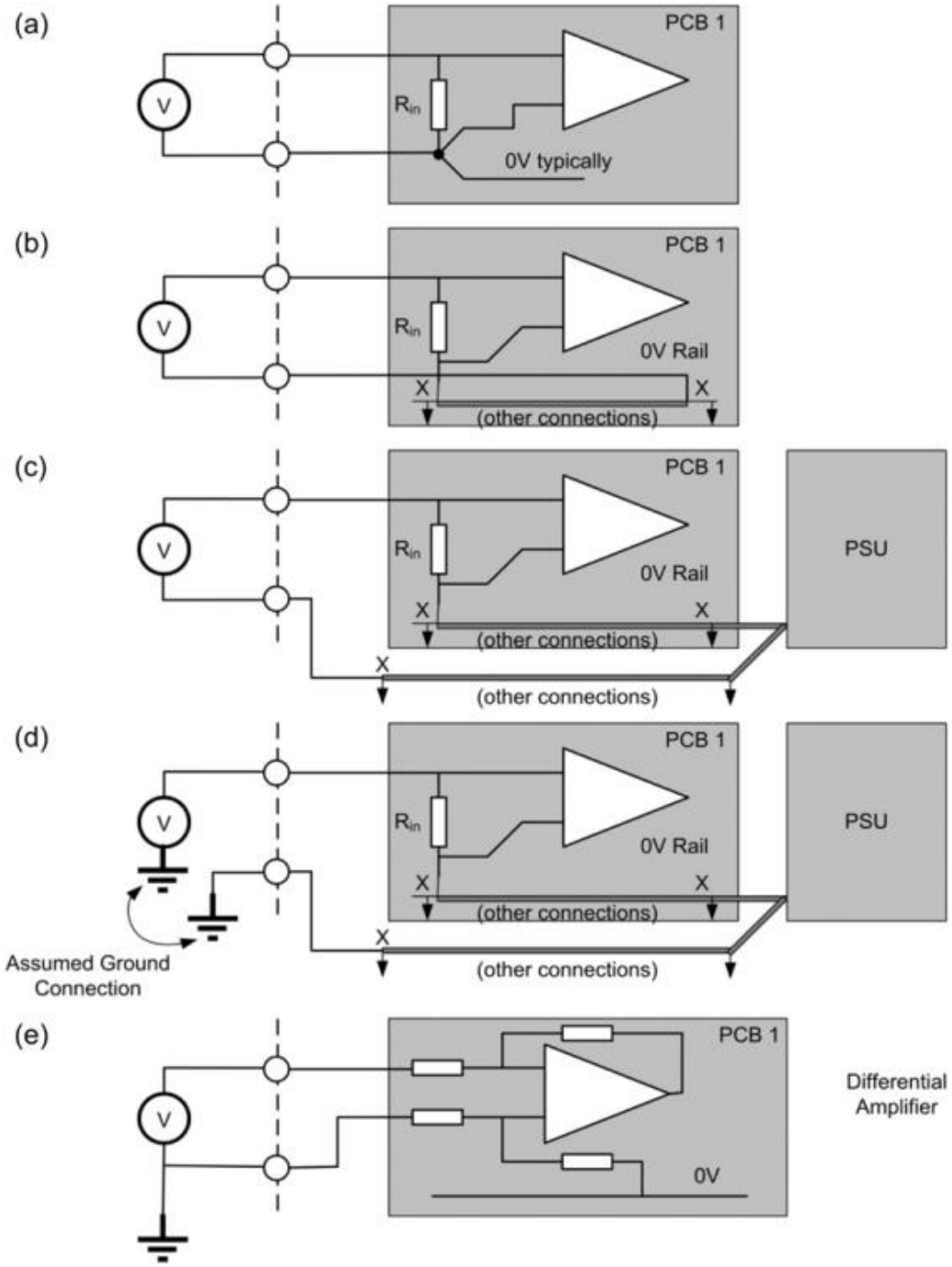

FIGURE 1.9 Input signal grounding

图 1.9:输入信号接地。

The reference point on a single-ended input is not always easy to find: look for the point from which the input voltage must be developed in order for the amplifier gain to act on it alone. In this way, no extra signals are introduced in series with the wanted signal by means of a common impedance. In each of the examples in Figure 1.9 of bad input wiring, getting progressively worse from (b) to (d), the impedance X - X acts as a source of unwanted input signal due to the other currents flowing in it as well as the input current.

找到单端输入上的参考点通常并不容易：输入电压必须在这个点上生成，以便放大器增益单独作用于这个点。这样，通过公共阻抗的方式就不会引入与有害信号串接在一起的额外信号。在图 1.9 的不良输入布线例子中，从(b)到(d)情况越来越糟糕，阻抗 X-X 将成为一个有害的输入信号源，因为除了输入电流外，还有其它电流在上面流动。

Connection to 0 V elsewhere on the PCB

Insufficient control over pc layout is the most usual cause of arrangement (b), especially if auto-routing layout software is used. Most CAD layout software assumes that the 0 V rail is a single node and feels itself free to make connections to it at any point along the track. To overcome this, either specify the input return point as a separate node and connect it later, or edit the final layout as required. Manual layout is capable of exactly the same mistake, although in this case it is due to lack of communication between designer and layout draughtsman.

连接到 PCB 上其它地方的 0V

对印刷电路版图控制的不充分是导致方案(b)的最常见理由，特别是如果使用了自动布线版图软件的时候。大多数 CAD 版图软件都假设 0V 轨是一个单节点，能够在走线的任何点连接 0V 轨。为了克服这个问题，要么将输入返回点规定为独立的节点，然后在以后连接，要么根据要求对最终版图进行编辑。人工设计版图也会犯完全相同的错误，虽然在这种情况下导致错误的原因是设计师和版图起草人之间缺少沟通。

Connection to 0 V within the unit

Arrangement (c) is quite often encountered if one pole of the input connector naturally makes contact with the metal case, such as happens with the standard BNC coaxial connector, or if for reasons of connector economy a common ground conductor is shared between multiple input, output or control signals that are distributed among different boards. With sensitive input signals, the latter is false economy; and if you have to use a BNC-type connector, you can get versions with insulating washers, or mount it on an insulating sub-panel in a hole in the metal enclosure.

连接到装置内的 0V

方案(c)也经常遇到，这种情况经常发生在输入连接器的一个极点自然地与金属外壳接触，比如使用标准 BNC 同轴连接器时发生的情况，或者由于节省连接器的原因，在分布于多块电路板的多个输入、输出或控制信号之间共享公共地导体之时。如果是敏感性高的输入信号，那么后者是错误的节约了。如果你必须使用 BNC 类型的连接器，你可以选用带绝缘垫圈的版本，或者将它安装在金属外壳孔洞中的绝缘子面板上。

Incidentally, taking a coax lead internally from an uninsulated BNC socket to the PCB, with the coax outer connected both to the BNC shell and the PCB 0V, will introduce a ground loop (see Section 1.1.4) unless it is the only path for ground currents to take. But at radio frequencies, this effect is countered by the ability of coax cable to concentrate the signal and return currents within the cable, so that the ground loop is only a problem at low frequencies.

还有种偶然的情况，那就是将同轴线从未绝缘的 BNC 插座经内部连接到 PCB，而同轴外壳与 BNC 外壳及 PCB 0V 连接在一起,这时会引入地环路(见 1.1.4 小节)，除非这是走地电流的唯一路径。但在射频频率时，这种效应会由于同轴电缆能够集中信号并在电缆内返回电流而解决，因此地环路只是低频时会出现的问题。

External ground connection

Despite being the most horrific input grounding scheme imaginable, arrangement (d) is unfortunately not rare. Now, not only are noise signals internal to the unit coupled into the signal path, but also all manner of external ground noise is included. Local earth differences of up to 50 Vat mains frequency can exist at particularly bad locations such as power stations, and differences of several volts are more common.

外部地连接

尽管方案(d)是可以想像的最可怕的输入接地方式,但不幸的是并不少见。现在，不仅装置内部的噪声信号会耦合进信号路径,而且所有方式的外部地噪声都包含在内。局部地电位差高达 50Vat 的工频会存在于特别糟糕的地方，比如发电站，而几伏的电位差较为常见。

The only conceivable reason to use this layout is if the input signal is already firmly tied to a remote ground outside the unit, and if this is the case it is far better to use a differential amplifier as in Figure 1.9(e), which is often the only workable solution for low-level signals and is in any case only a logical development of the correct approach for single-ended signals (a). If for some reason you are unable to take a ground return connection from the input signal, you will be stuck with ground-injected noise.

使用这种版图的唯一可以想到的理由是，输入信号已经被固定连接到装置外部的远程地。如果确实是这种情况，最好是使用图 1.9(e)中的差分放大器，对低电平信号来说这通常是唯一可行的解决方案，而且对单端信号来说是正确方法的合理演进(a)。如果由于某种原因你无法接受来自输入信号的地返回连接，那么你将遭受到地注入噪声。

All of the schemes of Figure 1.9(b) to (d) will work perfectly happily if the desired input signal is several orders of magnitude greater than the ground-injected interference, and this is frequently the case, which is how they came to be common practice in the first place. If there are good practical reasons for adopting them (for instance, connector or wiring cost restrictions) and you can be sure that interference levels will not be a problem, then do so. But you will need to have control over all possible connection paths before you can be sure that problems won't arise in the field.

如果目标输入信号的幅度比地注入干扰高好几个数量级，那么图 1.9(b)到(d)所示的所有方案都将完美工作，而这是经常发生的情况，也是它们最早成为习惯做法的原因。如果具有很好的实用性采纳理由(比如连接器或走线成本限制)，而且你能肯定干扰电平不是个问题，那么就这样做吧。但你在确保现场不会发生问题之前，你需要确保所有可能的连接路径都能受控。

1.1.7 Output signal ground

Similar precautions need to be taken with output signals, for the reverse reason. Inputs respond unfavorably to external interference, whereas outputs are the cause of interference. Usually in an electronic circuit there is some form of power amplification involved between input and output, so that an output will operate at a higher current level than an input, and there is therefore the possibility of unwanted feedback. The classical problem of output-to-input ground coupling is where both input and output share a common impedance, in the same way as the power rail common impedances discussed earlier. In this case the output current is made to circulate through the same conductor as connects the input signal return (Figure 1.10(a)).

图 1.1.7 输出信号地

基于相反的理由，输出信号也需要同样的防范措施。输入响应不利于外部干扰，而输出是干扰之源。通常在电子电路中，输入和输出之间存在某种形式的功率放大，因此输出将工作在比输入更高的电流值，因此存在有害反馈的可能性。

输出至输入接地耦合的经典问题是，输入和输出在哪里共享公共阻抗，这与前面讨论的电源轨公共阻抗是相同的方式。在这种情况下，输出电流将经过与输入信号返回连接相同的导体循环流动(图 1.10(a))。

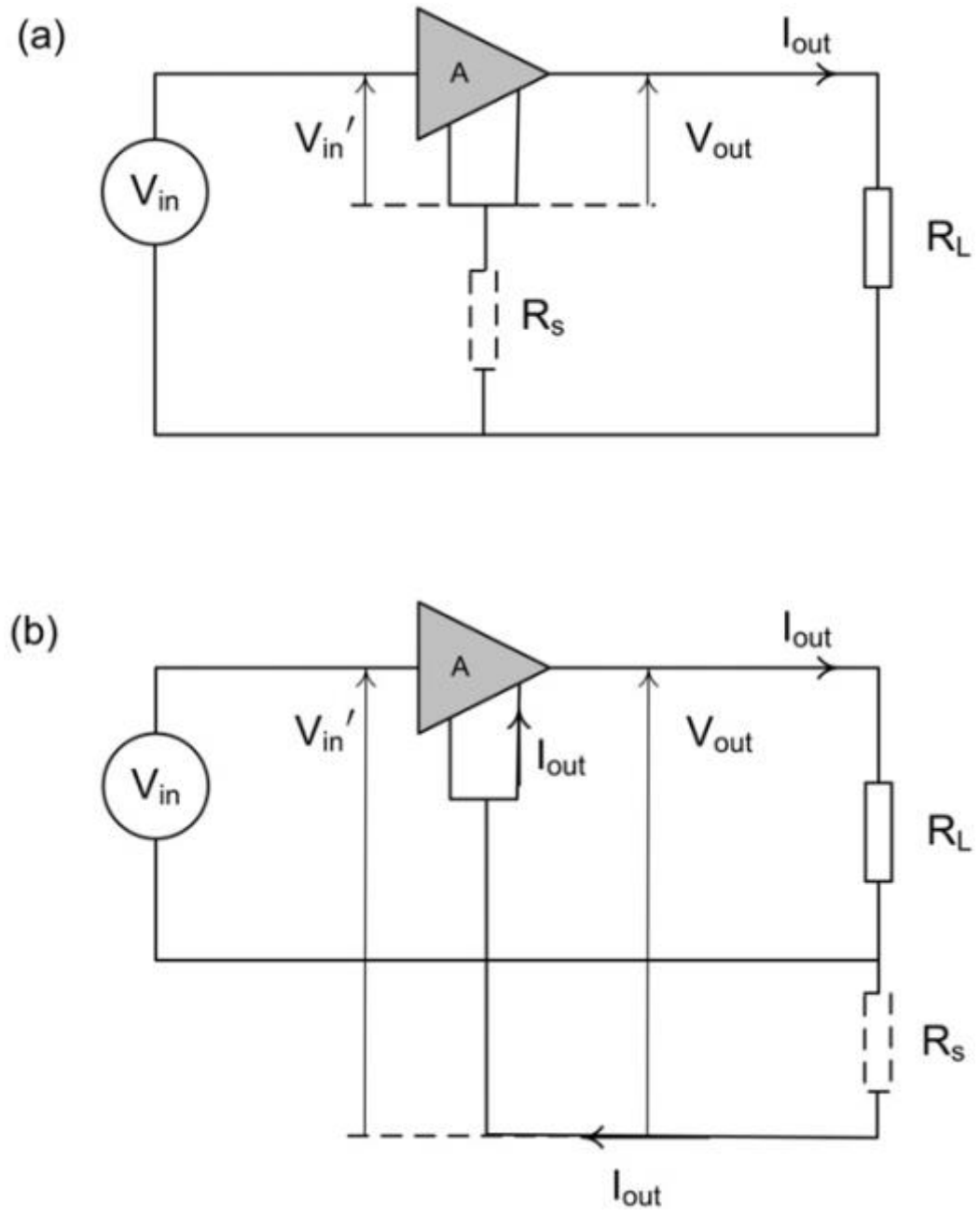

FIGURE 1.10 Output to input coupling

图 1.10 输出到输入耦合。

A tailor-made feedback mechanism has been inserted into this circuit, by means of R_S. The input voltage at the amplifier terminals is supposed to be V_{in}, but actually it is:

可将一种剪裁后的反馈机制通过 R_S 的方式插入这个电路。放大器端子处的输入电压应该是 V_{in}，但实际值为：

$$V_{in}' = V_{in} - (I_{out} \times R_S)$$

Redrawing the circuit to reference everything to the amplifier ground terminals (Figure 1.10(b)) shows this more clearly. When we work out the gain of this circuit, it turns out to be:

重新画这个电路，将所有对象都以放大器接地端子为参考(图 1.10(b))可以看得更清楚。这个电路的增益计算公式是：

$$V_{out}/V_{in} = A/(1 + [A \times R_S/(R_L + R_S)])$$

which describes a circuit that will oscillate if the term $[A \times R_S/(R_L + R_S)]$ is more negative than -1. In other words, for an inverting amplifier, the ratio of load impedance to common impedance must be less than the gain, to avoid instability.

这个公式表明，当$[A \times R_S/(R_L + R_S)]$这个项的值远小于-1 时，电路将发生振荡。换句话说，对于反相放大器而言，负载阻抗与公共阻抗之比必须小于增益才能避免出现不稳定性。

Even if the circuit remains stable, the extra coupling due to R_S upsets the expected response. Remember also that all the above terms vary with frequency, usually in a complex fashion, so that at high frequencies the response can be unpredictable. Note that although this has been presented in terms of an analog system (such as an audio amplifier), any system in which there is input - output gain will be similarly affected. This can apply equally to a digital system with an analog input and digital outputs which are controlled by it.

即使电路保持稳定状态，但由于 R_S 引起的额外耦合也会影响期望的响应。同时要记住，上面的所有项都会随频率而改变，而且改变方式非常复杂，因此在高频时的响应是不可预测的。注意，虽然这种现象存在于模拟系统方面(例如音频放大器)，但只要是有输入-输出增益的任何系统都会受到同样的影响。对于具有模拟输入和数字输出并且受控的数字系统来说这个理论同样成立。

Avoiding the common impedance

The preferable solution is to avoid the common impedance altogether by careful layout of input and output grounds. We have already looked at input grounds, and the grounding scheme for outputs is essentially similar: take the output ground return directly to the point from which output current is sourced, with no other connection (or at least, no other susceptible connection) in between.

避免公共阻抗

更好的解决方案是通过仔细设计输出和输出接地版图完全规避公共阻抗。我们已经讨论了输入接地，而输出接地方案实际上是相似的：将输出接地回路直接连到提供输出电流的点，两者之间再无其它连接(或至少没有其它易感连接)。

Normally, the output current comes from the power supply so the best solution is to take the return directly back to the supply. Thus the layout of PCB3 in Figure 1.2 should have a separate ground track for the high-current output as in Figure 1.11(a), or the high-current output terminal could be returned directly to the power supply, bypassing PCB3 (b).

正常情况下输出电流来自电源，因此最好的解决方案是将返回路径直接接回电源。这样图 1.2 中 PCB3 的版图应该像图 1.11(a)中那样给大电流输出提供一个独立的接地走线，或者大电流输出端子应绕过 PCB3 直接返回电源(b)。

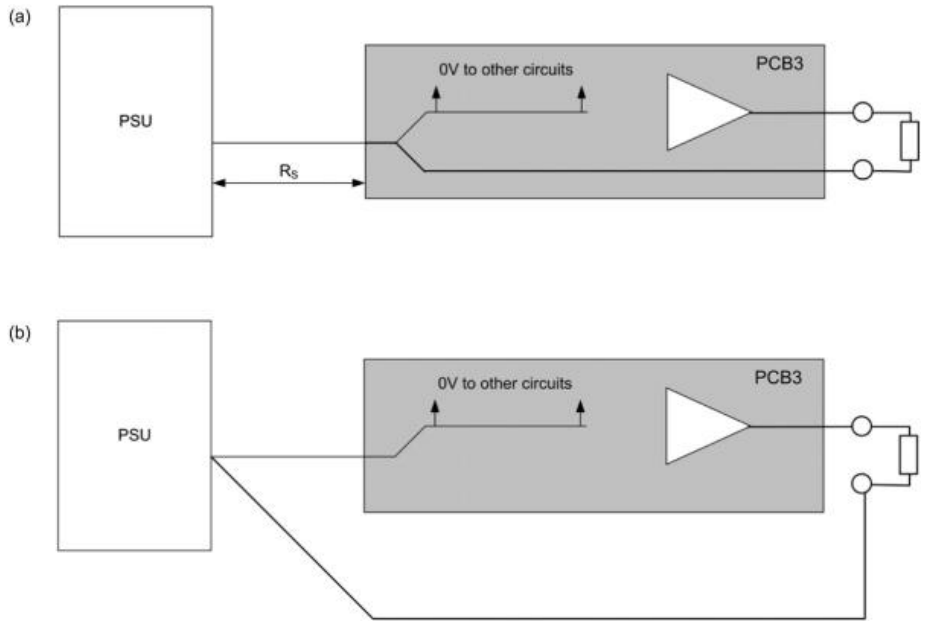

FIGURE 1.11 Output signal returns

图 1.11 输出信号返回路径。

If PCB3 contains only circuits which will not be susceptible to the voltage developed across R_S, then the first solution is acceptable. The important point is to decide in advance where your return currents will flow and ensure that they do not affect the operation of the rest of the circuits. This entails knowing the AC and DC impedance of any common connections, the magnitude and bandwidth of the output currents and the susceptibility of the potentially affected circuits.

如果 PCB3 只包含对 R_S 上产生的电压不敏感的电路，那么第一种解决方案是可以接受的。关键点是要提前确定返回电流将流向何方，并确保它们不影响其余电路

的工作。要做到这一点，必须分析理解任何公共连接的交流和直流阻抗、输出电流的幅度和带宽以及对可能受影响电路的易感性。